H.T.No. | | | | | | | | | | |

Code No: IT1502 **GEC-R14**

II B. Tech II Semester Supplementary Examinations, December 2017

COMPUTER ORGANIZATION

(Information Technology)

Time: 3 Hours **Max. Marks: 60**

Note: All Questions from **PART-A** are to be answered at one place.
Answer any **FOUR** questions from **PART-B.** All Questions carry equal Marks.

PART-A

6 × 2 = 12M

1. Explain the use of Program Counter and Instruction Register in CPU.
2. Define Micro-operations and Arithmetic Micro-operations.
3. Give the Micro Instruction format for the Control Memory.
4. List out the rules for floating point Addition and Subtraction.
5. Define i) Write Hit ii) Write Miss iii) Read Hit iv) Read Miss.
6. What is Cycle Stealing and Polling?

PART-B

4 × 12 = 48M

1. a) Explain various Bus Structures. (6M)
   b) Discuss about Error Detection Codes. (6M)
2. a) Draw and explain the block diagram of register organization with in CPU using common bus. (6M)
   b) Differentiate between RISC and CISC. (6M)
3. a) Discuss about the hardware configuration of a computer which is micro programmed. (8M)
   b) List out the Symbolic Micro Instructions needed for Fetch Routine. (4M)
4. a) Discuss about the working of 3-segmant RISC Pipeline. (6M)
   b) Draw the flowchart for floating point multiplication and explain with an example. (6M)
5. a) Explain Memory Hierarchy with a block diagram. (6M)
   b) Give the chip organization for SRAM and DRAM. (6M)
6. a) Explain Daisy Chain Priority Interrupt Handling. (6M)
   b) Draw and explain the block diagram of DMA Controller. (6M)

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