H.T.No. $\square$
Code No: EC1502
GEC-R14

## II B. Tech I Semester Supplementary Examinations, May 2016 SEMICONDUCTOR DEVICES AND CIRCUITS (Electrical and Electronics Engineering)

## Time: 3 Hours

Max. Marks: 60
Note: All Questions from PART-A are to be answered at one place.
Answer any FOUR questions from PART-B. All Questions carry equal Marks.

## PART-A

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6 \times 2=12 M
$$

1. Define Static resistance, dynamic resistance of a PN diode.
2. Draw the diagram associated in converting AC input to pure DC output \& explain the blocks.
3. The transistor has $I_{E}=10 \mathrm{~mA} \& \mathrm{a}=0.98$. Determine the value of $\mathrm{I}_{\mathrm{B}} \& \mathrm{I}_{\mathrm{C}}$.
4. What is thermal runaway? What is the condition for thermal stability?
5. Compare JFET with MOSFET.
6. Justify the validity of approximate hybrid model applicable in low frequency region.

## PART-B

$4 \times 12=48 M$

1. a) Explain V-I characteristics of a PN junction diode.
b) Explain the following
i) Open circuited PN junction.
ii) Varactor Diode.
2. a) Derive the expression for the ripple factor in a full wave rectifier using induction filter.
b) A zener diode shunt regulator circuit is to be designed to maintain a constant load current of 400 mA and voltage of 40 V .The input voltage is $90 \pm 5 \mathrm{~V}$. The zener diode voltage is 40 V and its dynamic resistance is $2.5 \Omega$.find the following quantities for the regulator: a) the series dropping resistance, b) zener power dissipation and c) load resistance. Assume the zener current to be $10 \%$ of load current.
3. a) Explain the V-I characteristics of UJT and also define intrinsic stand-off ratio.
b) Explain the two types of break down Mechanisms in detail?
4. a) A germanium transistor having $\beta=100$ and $\mathrm{V}_{\mathrm{BE}}=0.2 \mathrm{~V}$ is used in a fixed bias amplifier circuit where $\mathrm{V}_{\mathrm{CC}}=16 \mathrm{~V}, \mathrm{R}_{\mathrm{C}}=5 \mathrm{k} \Omega, \mathrm{R}_{\mathrm{B}}=790 \mathrm{k} \Omega$. Determine its operating point.
b) Draw a voltage divider bias circuit and derive an expression for its stability factor.
5. a) Explain the construction and operation of $N$ channel JFET with neat diagrams.
b) A FET has a driven current of 4 mA . If $\mathrm{I}_{\mathrm{DSS}}=8 \mathrm{~mA}$ and $\mathrm{V}_{\mathrm{GS}}$ (off) $=-6 \mathrm{~V}$. Find the values of $V_{G S} \& V_{P}$.
6. a) Determine $A_{I}, A_{V}, R_{I}$ and $R_{o}$ for a common collector circuit.
b) Explain the common source FET amplifier using small signal model. (6M)
