H.T.No. | | | | | | | | | | |

Code No: EC1515 **GEC-R14**

II B. Tech I Semester Regular / Suppl. Examinations, November 2017

DIGITAL CIRCUITS

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 60**

Note: All Questions from **PART-A** are to be answered at one place.
Answer any **FOUR** questions from **PART-B.** All Questions carry equal Marks.

PART-A

6 × 2 = 12M

1. What is 1's complement representation method?
2. Realize the EX-OR function using NAND gates.
3. Draw the full subtractor logic diagram using only 2-input NAND gates.
4. Explain emitter coupled logic.
5. Give the differences between synchronous and asynchronous counters.
6. What are the limitations of finite state machines?

PART-B

4 × 12 = 48M

1. a) Perform the following decimal subtractions in BCD by the 9's complement method.
   A) 448.3-242.2 B) 0345.5-453.7 (6M)
   b) The message below coded in the 7-bit hamming code is transmitted through a noisy channel. Decode the message assuming that at most a single error occurred in each code word. (6M)
   1001001,0111001,1000110,1100100
2. a) Design a binary to gray code converter using k-map. (6M)
   b) Reduce the following function using k-map
   $F(A,B,C,D) = \prod M(4,5,6,7,8,12,13)+d(1,15)$ (6M)
3. a) Explain carry look ahead adder circuit. (6M)
   b) Design a BCD adder circuit diagram. (6M)
4. a) Give the comparison of PROM, PLA and PAL. (6M)
   b) Explain transistor transistor logic in detail. (6M)
5. a) Design a decade counter using JK flip flop. (6M)
   b) Convert JK flip flop to D flip flop. (6M)

6. a) Determine a minimal state table equivalent to the state table given using partition method. (6M)

PS	NS,Z	
	X=0	X=1
A	E,0	D,1
B	F,0	D,0
C	E,0	B,1
D	F,0	B,0
E	C,0	F,1
F	B,0	C,0

b) Design a sequential circuit for the sequence detector 1110 using D flip-flops. (6M)

*****