H.T.No. | | | | | | | | | | |

Code No: CS1505 **GEC-R14**

II B. Tech II Semester Supplementary Examinations, June 2017

COMPUTER ORGANIZATION AND ARCHITECTURE

(Computer Science and Engineering)

Time: 3 Hours **Max. Marks: 60**

Note: All Questions from **PART-A** are to be answered at one place.
Answer any **FOUR** questions from **PART-B.** All Questions carry equal Marks.

PART-A

6 × 2 = 12M

1. a) List out the components of functional unit?
   b) What is the use of primary memory?
2. What is a microprogrammed control unit?
3. What is Signed-2's complement of -86?
4. What is memory hierarchy? Why do we need it?
5. Why does the DMA having priority over CPU when both requests for memory transfer.
6. Draw the structure of hypercube for n=2.

PART-B

4 × 12 = 48M

1. a) Design a bus system for connecting 4 registers each of size 4 bits. (6M)
   b) What are the different types of computer instructions? Explain how they are differentiated. (6M)
2. a) What is the difference between a microprocessor and a microprogram? (6M)
   b) What are the differences between hardwired control unit and micro programmed control unit. (6M)
3. a) Draw the flowchart for multiplication of Signed 2's complement data. (6M)
   b) Perform addition of BCD numbers 5439+6184 using all three methods. (6M)
4. a) Explain Associative and Set-Associative mapping techniques of Cache memory. (6M)
   b) Write shorts notes on main memory and explain how it is connected to CPU. (6M)

5. a) Distinguish between memory mapped I/O and Isolated I/O. (6M)

   b) Explain bit oriented protocol. (6M)

6. Explain the following with examples.

   i) Delayed Branches (6M)

   ii) Dynamic Branch Prediction. (6M)

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