H.T.No. | | | | | | | | | | |

Code No: CT1505 **GEC-R14**

II B.Tech I Semester Regular Examinations, November 2016

DIGITAL LOGIC DESIGN

(Common to Computer Science and Engineering & Information Technology)

Time: 3 Hours **Max. Marks: 60**

Note: All Questions from **PART-A** are to be answered at one place.
Answer any **FOUR** questions from **PART-B.** All Questions carry equal Marks.

PART-A

6 × 2 = 12M

1. Convert $(123)_{10}$ into ($)_6$?
2. State the Duality principle with example.
3. Compare serial adder and parallel adder
4. What is Encoder? Give an example.
5. Give the Excitation table of S-R flip-flop.
6. Differentiate between synchronous and asynchronous counters.

PART-B

4 × 12 = 48M

1. a) Convert the following

   i) $(643.512)_{10}$ to excess-3 code ii) $(96.42)_{10}$ to BCD code

   iii) Gray code (110101) into binary code (6M)

   b) Perform the following operations using 2's complement method

   i) $(1010)_2 - (1111)_2$ ii) $(1010)_2 - (1000)_2$

   iii) $(001110)_2+(110010)_2$ (6M)

2. a) Express the following functions in sum of min-terms and product of max-terms.

   i) (xy+z) (y+xz)

   ii) B^1D+A^1D+BD (6M)

   b) Simplify the following Boolean function using K-map
   $F(W,X,Y,Z)=\sum(1,4,5,6,12,14,15)$ (6M)

3. a) With the help of logic diagram and example explain 4-bit ripple adder/ subtractor using 2's complement method. (8M)

   b) Design Half Subtractor. (4M)

4. a) Implement 16X1 multiplexer by using two 8X1 multiplexers and one 2X1 multiplexer. (6M)

   b) Implement the following Boolean functions using Decoder and OR gate
   $F_1(A,B,C) = \sum(3,5,6)$

   $F_2(A,B,C) = \sum(1,4)$

   $F_3(A,B,C) = \sum(2,3,5,6)$ (6M)

5. a) Convert a J-K flip-flop into D Flip-flop (6M)

   b) Draw the circuit diagram of J-K flip flop with NAND gates explain its operation with the help of a truth table. (6M)

6. a) Explain in detail about Universal Shift Register (7M)

   b) Design mod-6 counter (5M)

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