Code No: 126EN **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year II Semester Examinations, April - 2018

VLSI DESIGN

(Common to ECE, ETM)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a) Define figure of merit of MOS transistor. [2]
b) Draw the CMOS inverter circuit. [3]
c) What is meant by synthesis? [2]
d) Differentiate Functional simulation and timing simulation. [3]
e) What is the importance of fan-in and fan-out? [2]
f) Differentiate rise time and fall time. [3]
g) Draw the 1-bit SRAM cell. [2]
h) What are the various serial access memories? [3]
i) Implement 2:1 MUX using PAL. [2]
j) What is the difference between verification and validation? [3]

PART - B

(50 Marks)

2. Draw and explain the operation of BiCMOS inverter. [10]

OR

3. Derive the drain to source current equation for NMOS enhancement mode transistor. [10]

4. Discuss the steps involved in VLSI design flow. [10]

OR

5. Draw the stick diagram for the following Boolean expression using CMOS logic. $F = A(B + C)$. [10]

6. Briefly explain the commonly used technique to estimate the delay time of a MOS inverter. [10]

OR

7. Implement 4:1 multiplexer using switch logic. [10]

8. Design a 4-bit magnitude comparator. [10]

OR

9. Design a zero detector circuit. [10]

10. Discuss scan design Techniques. [10]

OR

11. Compare various programmable devices. [10]

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