Code No: 115EB **R13**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech III Year I Semester Examinations, November/December - 2016
LINEAR AND DIGITAL IC APPLICATIONS
(Common to ECE, ETM)

Time: 3 hours **Max. Marks: 75**

Note: This question paper contains two parts A and B.
Part A is compulsory which carries 25 marks. Answer all questions in Part A. Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

PART - A

(25 Marks)

1.a)	Define unity gain band width of an op-amp.	[2]
b)	Define slew rate. What causes it?	[3]
c)	What is switched capacitor filter?	[2]
d)	Draw the circuit diagram of AM detector using PLL.	[3]
e)	Which type of ADC is the fastest? Why?	[2]
f)	An 8 bit DAC has a resolution of 20mv/bit. What is analog output voltage?	[3]
g)	Mention any two applications of multiplier IC.	[2]
h)	Realize EX-OR gate with CMOS circuit.	[3]
i)	Write the difference between static and dynamic RAM's.	[2]
j)	Draw the block diagram of 3-bit ring counter.	[3]

PART - B

(50 Marks)

2. With neat circuit diagram explain the operation of Schmitt trigger. [10]

OR

3.a) An IC op-amp 741 used as an inverting amplifier with a gain of 100. The voltage gain vs frequency characteristic is flat up to 12 kHz. Find the maximum peak to peak input signal that can be feed without causing any distortion to the output.

b) Draw and explain the output waveform of the ideal inverter circuit when the input is square wave. [5+5]

4. Explain the operation of mono stable multi vibrator using 555 timers. Derive the expression of time delay of mono stable multi vibrator with 555 timers. [10]

OR

5.a) From the given component values find the free running frequency. Control voltage Vc=10.9v, Vcc=12v, R1=4.7k and C1=1.1Nf.

b) Design a narrow band bandpass filter using op-amp. The resonant frequency is 100HZ and Q=2. Assume c=0.1Uf. [5+5]

6. Draw the schematic block diagram of dual slop A/D converter and explain its operation. Derive expression for its output voltage. [10]

OR

7.a) What are the limitations of weighted resistor type D/A converter?

b) What do you mean by quantization error in an A/D converter? [5+5]

8. Find the state diagram and state table of a binary coded decimal to excess-3 decoder. [10]

OR

9. Draw the basic DTL gate and explain its operation. [10]

10.a) Design a 4 to 16 decoder using two 74×138 IC's.

b) Implement the following Boolean expression using 74×151 IC F(z)=AB+BC+AC. [5+5]

OR

11. With the help of timing diagram explain read and write operations of SRAM. [10]

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