H.T.No. | | | | | | | | | | |

Code No: EC1919 **GEC-R14**

M. Tech II Semester Regular/Suppl. Examinations, July 2017

LOW POWER VLSI DESIGN

(Digital Electronics and Communication Systems)

Time: 3 Hours **Max. Marks: 60**

Note: Answer any **FIVE** questions. All Questions carry equal Marks.

5 × 12 = 60M

1. a) Explain about different sources of power dissipation in digital CMOS circuit. (6M)

   b) Explain design limitations of low voltage, low power circuits. (6M)

2. a) Describe the Low – Voltage, Low- power CMOS SOI process. (6M)

   b) Explain about the advanced isolation technologies related to BiCMOS. (6M)

3. a) What is the need of Graded-Drain structure? Explain about double-diffused drain technique. (6M)

   b) Explain about Retrograde-Well CMOS technology. (6M)

4. a) Explain about low voltage, low power design technique for adder circuits. (6M)

   b) Explain about Wallace tree multiplier and compare its power requirement with reference to other multipliers. (6M)

5. a) Explain the need for low power latches & flip-flops and their major uses. (6M)

   b) Explain the pipelining theme used to produce fast flip-flop structures. (6M)

6. a) What is the use of self-refresh circuit in DRAM? Explain the operation of 3 transistor DRAM cell with required waveforms. (6M)

   b) What is the need and advantage of Floating Gate memory device? (6M)

7. a) Design and explain double edge triggered flip-flop. (6M)

   b) Explain the operation of a 4T RAM cell. (6M)

8. Explain how both the multipliers can be treated as low voltage, low power architectures

   i) Baugh- Wooley multiplier. (6M)

   ii) Booth Multiplier. (6M)

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