H.T.No. | | | | | | | | | | |

EC1919 **GEC-R14**

M. Tech II Semester Regular/Suppl. Examinations, July 2016

LOW POWER VLSI DESIGN

(Digital Electronics & Communication Systems)

Time: 3 Hours **Max. Marks: 60**

Note: Answer any **FIVE** questions. All Questions carry equal Marks.

5 × 12 = 60M

1. a) Explain different sources of power dissipation in digital CMOS circuit. (6M)

   b) Briefly outline the needs for low power VLSI chips. (6M)

2. a) Explain BICMOS processes with neat sketches (6M)

   b) Explain integrated analog/digital CMOS process (6M)

3. Write short notes on:

   a) Standard adder cells (6M)

   b) Low voltage low power design techniques (6M)

4. Explain the multiplier architectures of Braun and Baugh-Wooley with example (12M)

5. a) Explain about evaluation of flip-flops with an example (6M)

   b) Briefly describe quality measures of Latches and flip-flops (6M)

6. Design any low power combinational circuit and evaluate its power. (12M)

7. Draw and explain the operation of 4T SRAM cell and 6T SRAM cell. (12M)

8. a) Explain about future trends and developments of DRAM (6M)

   b) Explain the operation of self-refresh circuit with neat diagram (6M)

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