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Code No: EC1515

GEC-R14

II B. Tech II Semester Regular Examinations, April 2017

**DIGITAL CIRCUITS**  
(Electrical and Electronics Engineering)

Time: 3 Hours

Max. Marks: 60

**Note:** All Questions from **PART-A** are to be answered at one place.

Answer any **FOUR** questions from **PART-B**. All Questions carry equal Marks.

**PART-A**

**6 × 2 = 12M**

1. What is the largest positive number that can be stored in a computer that has 16-bit word length and uses 2's complement arithmetic?
2. Draw the logical gates diagram for  $X = (AB) \cdot (\overline{A + B}) + \overline{EF}$ .
3. a) What is the function of comparator?  
b) What is encoding?
4. What are the advantages of ROM using as a PLD?
5. Define setup time and Hold time.
6. What are the capabilities of finite state machines?

**PART-B**

**4 × 12 = 48M**

1. a) Convert decimal 8.723 to both Hex and octal codes. (6M)  
b) Express decimal digits 0-9 in BCD code and 2-4-2-1 code. Determine which of the above codes are self-complementing. (6M)
2. a) Minimize following function using Tabular minimization.  
 $F(A, B, C, D) = \sum m(6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$ . (8M)  
b) What are the advantages and disadvantages of the tabular method compared to K-map? (4M)
3. a) Design a full adder with two half adders and OR gate. (4M)  
b) Design an Excess-3 adder using 4-bit parallel binary adder and logic gates. (8M)
4. a) Draw and explain the CMOS circuit from the expression  $Y = A'B + C$ . (6M)  
b) Give the description of CMOS 2 input AND gate and its circuit diagram. (6M)

5. a) Explain the following terms in connection with a flip-flop (6M)
- i) Preset
  - ii) Clear
  - iii) Race-around condition
- b) Draw the schematic circuit of Toggle flip-flop (T). Give its truth-table. Justify the entries in the truth-table. (NAND gates only). (6M)
6. Realize the 4-bit serial binary adder using D flip flops and Mealy FSM. (12M)

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