H.T.No. | | | | | | | | | | |

Code No: EC1534 **GEC-R14**

III B. Tech II Semester Supplementary Examinations, November 2017

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 60**

Note: All Questions from **PART-A** are to be answered at one place.
Answer any **FOUR** questions from **Part-B.** All Questions carry equal Marks.

PART-A

6 × 2 = 12M

1. Draw the structure of P-well process CMOS transistor.
2. Define latch-up.
3. What are the various MOS layers used to design a Transistors?
4. What is area capacitance and write the units of area capacitance?
5. Write any two advantages and disadvantages of PLA's.
6. Draw the RTL simulation flow.

PART-B

4 × 12 = 48M

1. Draw and explain the fabrication process steps involved in nMOS transistor. (12M)
2. Determine pull-up to pull-down ratio for nMOS inverter driven by another nMOS inverter with one or more pass transistors. (12M)
3. Explain about Micron based design rules and its significance. (12M)
4. Explain how to estimate the rise time and fall time in a CMOS inverter with suitable MOS models. (12M)
5. Draw the general arrangement of 4-bit Arithmetic Processor and explain the function of each block in detail. (12M)
6. a) Explain in detail about place and route in high level VLSI design. (6M)
   b) Implement a Full adder using half adders and write VHDL code in data flow model. (6M)

*****