H.T.No. | | | | | | | | | | |

Code No: EC1534 **GEC-R14**

III B. Tech II Semester Regular Examinations, April 2017

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 60**

Note: All Questions from **PART-A** are to be answered at one place.
Answer any **FOUR** questions from **PART-B.** All Questions carry equal Marks.

PART-A

6 × 2 = 12M

1. Classify ICs based on transistor count.
2. Draw the CMOS Inverter circuit.
3. What is Layout diagram of a PMOS Transistor?
4. What is the significance of scaling in VLSI technology?
5. How a Barrel shifter is different from general shifter?
6. What are the advantages of HDL based designs?

PART-B

4 × 12 = 48M

1. Draw and explain the fabrication process of NMOS Transistor. (12M)
2. Determine pull-up to pull-down ratio for nMOS inverter driven by another nMOS inverter with one or more pass transistors (12M)
3. a) Draw the layout for EX-OR gate using CMOS logic. (6M)
   b) Design a layout diagram for $Y = (A+B+C+D)^I$ using NMOS logic. (6M)
4. a) Write short notes on standard and area capacitances. (6M)
   b) Calculate ON resistance of the NMOS inverter from V_{DD} to GND if n-channel sheet resistance $R_{sn}=10^4\Omega$ per square and p-channel sheet resistance $R_{sp}=2.5 \times 10^4\Omega$ per square and Zpu/Zpd = 4:1. (6M)
5. a) What are the general considerations in Sub System Design Process? (5M)
   b) Write short notes on PLDs with examples. (7M)
6. a) What is meant by RTL simulation and explain? (6M)
   b) Write a VHDL program for D-flip-flop using behavioral style of modeling. (6M)

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