H.T.No. | | | | | | | | | | |

Code No: EC1527 **GEC-R14**

III B. Tech I Semester Supplementary Examinations, July 2017

LINEAR AND DIGITAL ICs

(Electronics and Communication Engineering)

Time: 3 Hours **Max. Marks: 60**

Note: All Questions from **PART-A** are to be answered at one place.
Answer any **FOUR** questions from **PART-B.** All Questions carry equal Marks.

PART-A

6 × 2 = 12M

1. Draw an equivalent circuit and list out various Ideal and Practical specifications of an op-amp.
2. Obtain open loop and closed loop gain expression for an inverting and non-inverting amplifier.
3. Write the difference between two types of ADCs.
4. Derive the voltage to frequency conversion factor for VCO.
5. Draw the logic symbol and truth table for IC 74×139.
6. Sketch 1-bit DRAM cell and explain its operation.

PART-B

4 × 12 = 48M

1. a) With neat diagram, explain the functionality of each basic building blocks of an op-amp. (6M)
   b) Develop gain versus frequency response curves for external frequency compensation with different slope decades. (6M)
2. a) Derive the V_O expression for ANTI LOG amplifier using IC741. (6M)
   b) Explain how an op-amp can be used for converting V to I and I to V. (6M)
3. a) Design R-2R ladder DAC circuit using IC741 and explain its operation. (6M)
   b) Explain the operation of SAR-ADC technique with suitable example. (6M)
4. a) Derive the Time period oscillations expression for monostable multi vibrator using IC555. (6M)
   b) Explain about various blocks used in PLL and derive the equation for error voltage V_e. (6M)

5. a) Draw the logic diagram of IC 74×283 and design a 24-bit ripple adder using the same IC. (6M)

   b) Design a modulo 100 counter using two 74x163 binary counters. (6M)

6. a) Explain various timing parameters and applications of ROM. (6M)

   b) Draw an internal structure of SRAM and explain its operation. (6M)

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