H.T.No. | | | | | | | | | | |

Code No: CT1505 **GEC-R14**

II B. Tech I Semester Regular / Suppl. Examinations, November 2017

DIGITAL LOGIC DESIGN

(Common to Computer Science and Engineering and Information Technology)

Time: 3 Hours **Max. Marks: 60**

Note: All Questions from **PART-A** are to be answered at one place.
Answer any **FOUR** questions from **PART-B.** All Questions carry equal Marks.

PART-A

6 × 2 = 12M

1. Given the two binary numbers X=1010100 and Y=1000011, perform the subtraction X-Y by using 2's complement.
2. Implement the Boolean function F = xy+x'y'+y'z with AND, OR and inverter gates.
3. Draw the logic diagram of Half adder.
4. Draw the logic diagram of 4X16 decoder constructed with two 3X8 Decoders with enable input.
5. Differentiate Latch and Flip flop.
6. Draw the logic diagram of a BCD ripple counter constructed from a four-bit binary ripple counter with asynchronous clear and NAND gate that detects the occurrence of count 1010.

PART-B

4 × 12 = 48M

1. a) Find i) 16's complement of B2FA.
   ii) 9's Complement of 5,137 (4M)

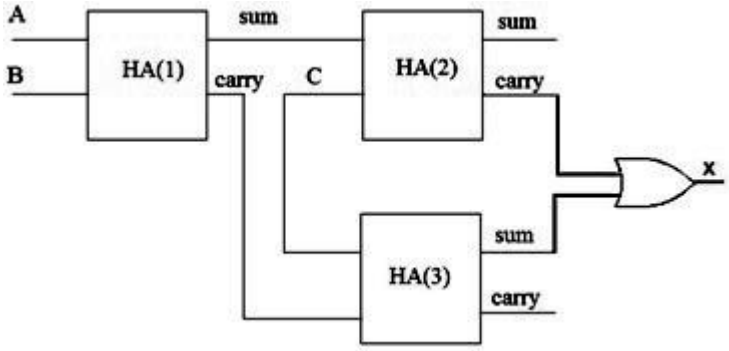
   b) i) Convert the hexadecimal number 68BE to binary, and then convert it from binary to octal.

   ii) Add the following numbers without converting them to decimal. (8M)
   Binary numbers 1011 and 101
   Hexadecimal numbers 2E and 34

2. a) Using K-map, simplify the Boolean function F=XY, to represent in SOP form where
   X(A,B,C,D)=ABC'+C'D+A'CD'+B'CD'
   Y(A,B,C,D)=(A+B+C'+D')(B'+C'+D)(A'+C+D') (6M)

   b) Simplify the Boolean function F, together with the don't-care conditions d as given below
   F(A,B,C,D)=Σ(4,5,7,12,13,14)
   d(A,B,C,D)=Σ(9,11,15) using k-map (6M)

3. a) Obtain the Boolean expression for the output (sum, carry and x) of the following logic circuit. (6M)



b) Implement a Full adder circuit using only NAND gates. (6M)

4. a) Obtain the PLA programming table and logic diagram of a full adder. (6M)

b) Implement a Full adder circuit with a decoder. The adder inputs are A, B & C. The adder produces outputs S and C_0. (6M)

5. a) Draw and explain the SR-latch using NAND and NOR Gates with suitable tables. (6M)

b) Draw the schematic circuit of JK Flip-Flop with negative edge triggering and explain the operation (6M)

6. a) Design a synchronous Modulo-6 counter using JK Flip-flops and NAND gates. (6M)

b) Design a 4-bit binary ripple counter with JK Flip-flops. (6M)

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