H.T.No. | | | | | | | | | | |

Code No: CT1505 **GEC-R14**

II B. Tech I Semester Supplementary Examinations, June 2017

DIGITAL LOGIC DESIGN

(Common to Computer Science and Engineering and Information Technology)

Time: 3 Hours **Max. Marks: 60**

Note: All Questions from **PART-A** are to be answered at one place.
Answer any **FOUR** questions from **PART-B.** All Questions carry equal Marks.

PART-A

6 × 2 = 12M

1. Distinguish between 1's complement and 2's complement numbers.
2. Explain minimal SOP and POS forms?
3. Draw the truth table of Full Adder?
4. Realize 1-to-4 demultiplexer using 1-to-2 demultiplexers.
5. Realize a T Flip Flop using D Flip Flop?
6. List the applications of registers.

PART-B

4 × 12 = 48M

1. a) Solve for X. (6M)

   i) $(789)_{16} + (478)_8 = (X)_4$ ii) $(4085.025)_{10} = (X)_{15}$

   b) Convert the following numbers. (6M)

   i) $(1984)_{10}$ to base 8 ii) $(53.1575)_{10}$ to base 2 iii) $(3A6)_{16}$ to decimal

2. a) Realize all basic logic gates using universal gates. (6M)

   b) Simplify the following Boolean functions using Karnaugh maps to a minimum number of terms. (6M)

   i) $F(A,B,C,D) = \sum m(0,1,2,4,6,9,10)$ ii) $F(a,b.c) = \sum m(1,2,5,7) + d(0)$

3. a) Draw the diagram for a 4 bit adder/subtractor circuit and explain its operation. (6M)

   b) Construct a full adder using XOR and NAND gates only. (6M)

4. a) Implement Full Adder circuit using PAL? (6M)

   b) Realize a 4-bit BCD to Gray Code converter using PLA? (6M)

5. a) Explain any 2 Flip Flops using Truth tables and Excitation Tables. (6M)

   b) Design a Synchronous Decade Counter using D Flip Flop? (6M)

6. a) Draw the diagram of universal shift register and explain in detail. (6M)

   b) Draw and explain in detail about 4-bit Johnson Counter. (6M)

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